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AMENDEMENT 1
AMENDMENT 1

1999-01

Amendment 1

**VMEbus –
Microprocessor system bus
for 1 byte to 4 byte data**

Amendement 1

*Bus VMEbus –
Bus système à microprocesseurs
pour données de 1 octet à 4 octets*

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FOREWORD

This amendment has been prepared by subcommittee 26: Microprocessor systems, of the Joint Technical Committee ISO/IEC JTC 1: Information technology.

The text of this amendment is based on the following documents:

Text	Report on voting
ISO/IEC JTC1/SC 26 N 237	ISO/IEC JTC1/SC 26 N 218

Full information the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

CHAPTER 2: IEC 60821 BUS DATA TRANSFER BUS

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2.2.4.5 WRITE*

Replace the first sentence of this subclause by the following:

WRITE* is a level significant signal line that is strobed by the falling edge of the first data strobe (DSA*) and is valid as long as any data strobe (DSA* or DSB*) is low.

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2.3.6 Basic data transfer capabilities

Replace Rule 2.65 by the following:

D08(O) SLAVES MUST NOT respond by driving DTACK* low during cycles that request access to byte locations BYTE(0), BYTE(2), BYTE(1-2), BYTE(2-3), BYTE(0-2), BYTE(1-3), or BYTE(0-3).

Insert, at the end of Suggestion 2.8, the following text:

4) When a D08(O) SLAVE is requested to do a BYTE(0) or BYTE(2) transfer.

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Table 2-10 – Mnemonics that specify basic data transfer capabilities

Replace in the third column the words "can accept" and "can monitor" by "must accept" and "must monitor".