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**Information technology—
Microprocessor systems—
High-performance synchronous 32-bit bus:
MULTIBUS II**

*Technologies de l'information –
Systèmes à microprocesseurs –
Bus 32 bits synchrone à haute performance:
MULTIBUS II*



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Abstract: The operation, functions, and attributes of a parallel system bus (PSB), called MULTIBUS II, are defined. A high-performance backplane bus intended for use in multiple processor systems, the PSB incorporates synchronous, 32-bit multiplexed address/data, with error detection, and uses a 10 MHz bus clock. This design is intended to provide reliable state-of-the-art operation and to allow the implementation of cost-effective, high-performance VLSI for the bus interface. Memory, I/O, message, and geographic address spaces are defined. Error detection and retry are provided for messages. The message-passing design allows a VLSI implementation, so that virtually all modules on the bus will utilize the bus at its highest performance—32 to 40 Mbyte/s. An overview of PSB, signal descriptions, the PSB protocol, electrical characteristics, and mechanical specifications are covered.

Keywords: high-performance synchronous 32-bit bus, MULTIBUS II, system bus architectures

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